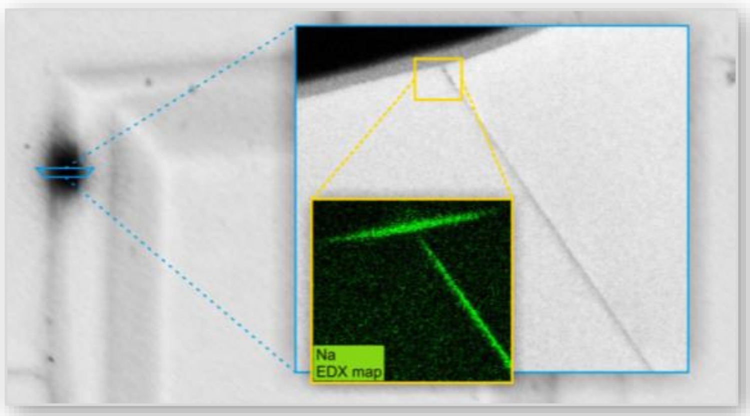
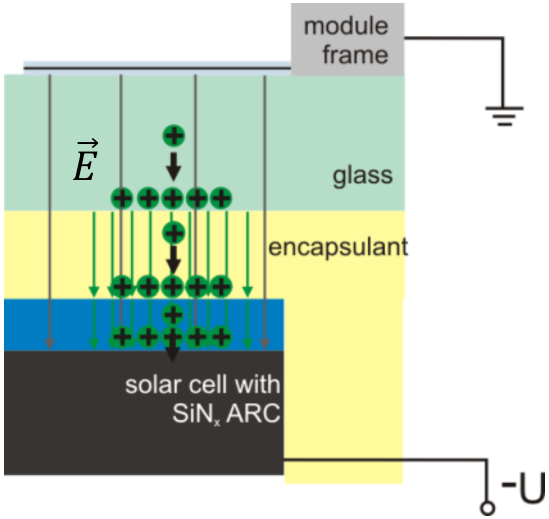
PID-shunting:
Understanding from nanoscale to module level

PV Module Reliability Workshop 2014-02-25





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Outline

- Introduction: Potential-induced degradation of shunting type (PID-s)
- PID test for unlaminated solar cells and encapsulants
- The nature of PID-shunts
  - Local shunts
  - High resolution defect analysis
- Voltage divider model for solar module encapsulation
  - Measurement of leakage currents and voltage distribution
  - Explanation of approaches for PID prevention

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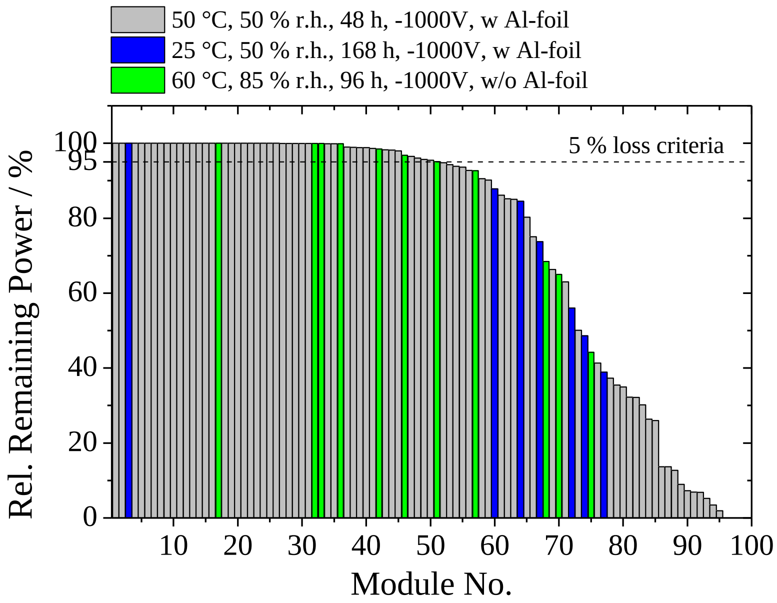
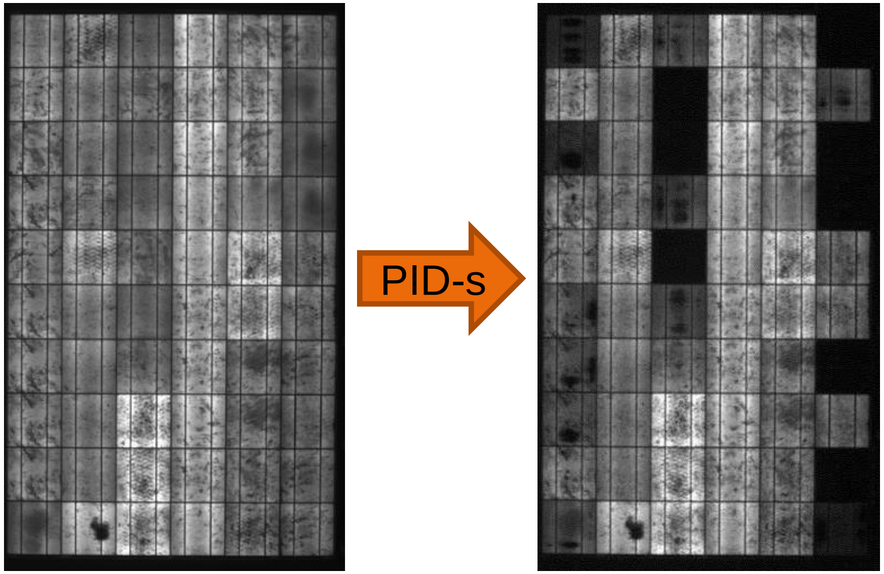
Potential-induced degradation of shunting type (PID-s)

- Large potential between front glass surface and solar cells
  → leakage current (cations, electrons) [1, 2]
- Massive reduction of the parallel resistance = shunting → PID-s
- Great efforts to achieve a test standard require a basic understanding



Relative power output after PID tests at 95 modules

S. Dietrich et al., Experiences on PID testing of PV modules in 2012, NREL PV Module Reliability Workshop 2013



Electroluminescence imaging reveals PID-s

[1] P. Hacke et al., Proc. of 25th EU-PVSEC, Valencia, Spain, 2010
[2] S. Pingel et al., Proc. of 35th IEEE PVSC, Honolulu, USA, 2010

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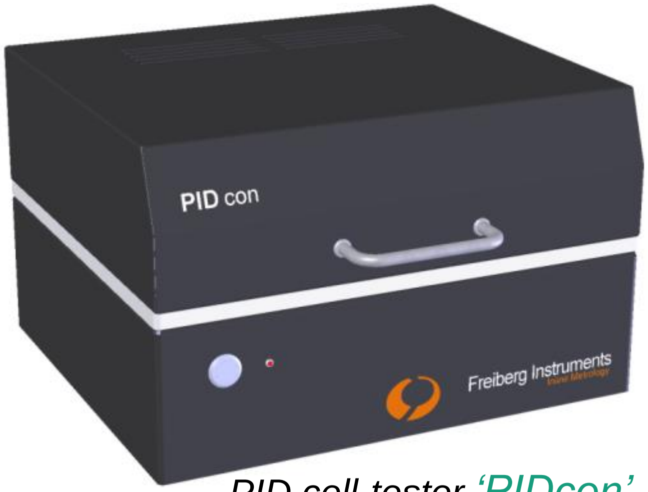
PID test for unlaminated solar cells and encapsulants

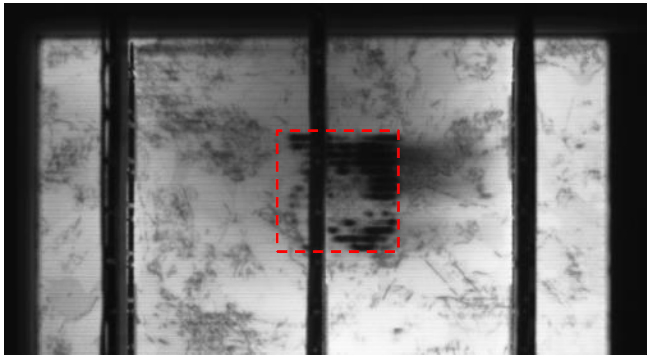
- PID test procedure for solar cells and module components (glass, polymer sheets)
- Use of standard encapsulation materials
- PID-testing without manufacturing of mini modules, no climate chamber necessary
- In-situ recording of R_p
- Patent pending
- Commercially available (Freiberg Instruments/Germany)

→ Fast and inexpensive quality check for cells

→ Flexible tool for R&D (cells, encapsulants)



PID cell-tester 'PIDcon'



EL image of a multicrystalline Si solar cell after PID test on an area of 4x4 cm² (shunted region)

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Comparison of PID test methods

	Time to result	Closeness to reality	Varia-bility	Control of test	Cost per test (incl. equipment)
In-field testing					
- 'intelligent' HV source	−−	++	o	o	−−
- permanent HV	−	+	o	+	−
Climate chamber					
- Standard modules	o	+	+	++	−−
- Mini modules	+	o	+	++	o
Corona test					
- of mini modules	+	o	+	−	+
- unlaminated solar cells	++	−−	−	−	++
PIDcon cell test	**+**	**o**	**+**	**+**	**++**

V. Naumann et al., NREL PV Module Reliability Workshop 2014

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Physical nature of PID-shunts

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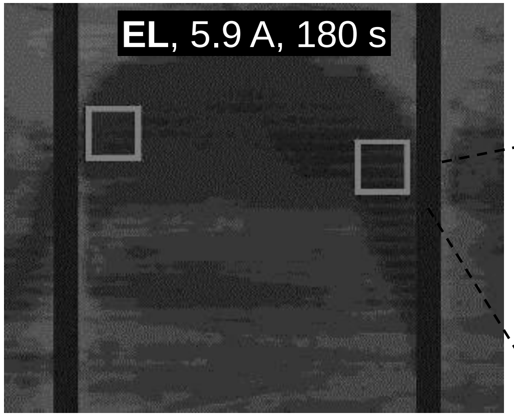
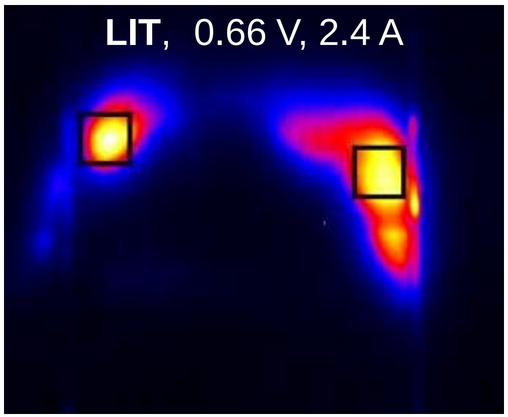
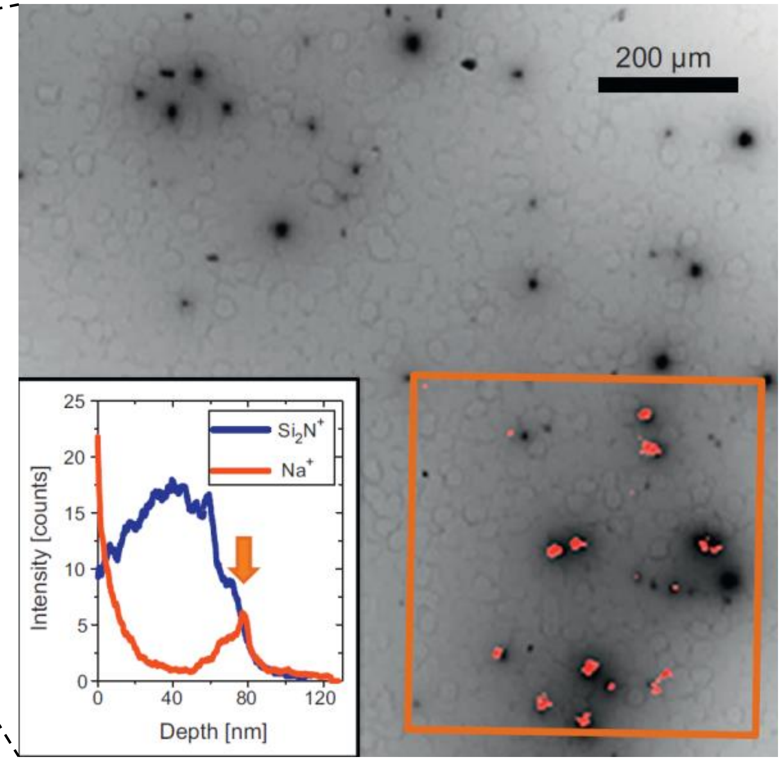
Physical nature of PID-shunts: local shunts





Imaging of local PID-shunts with SEM/EBIC*



*Electron Beam Induced Current

ToF-SIMS Na^+-map

- PID-shunted regions consist of high numbers of local shunts
- Accumulations of Na at the SiN_x-Si interface correlate with shunt positions

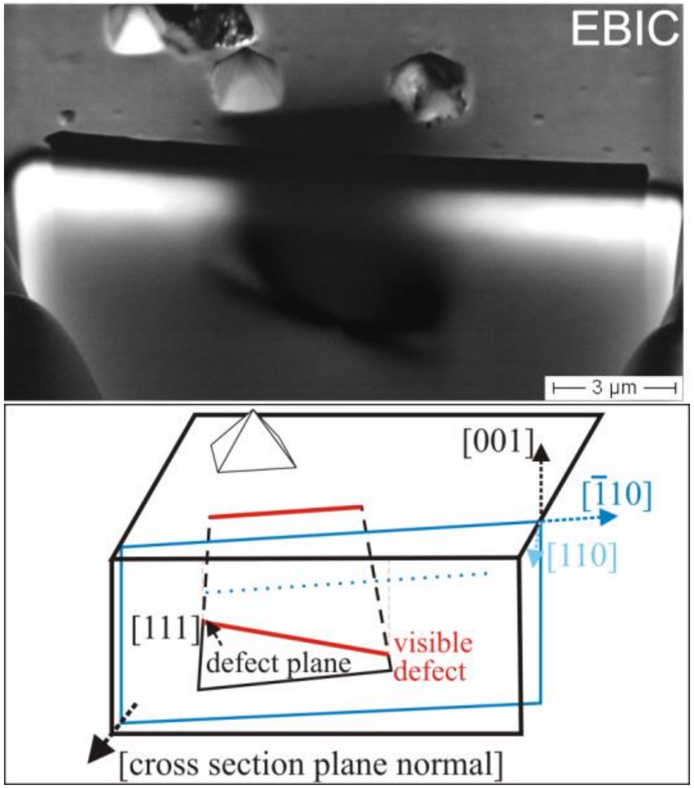
[1] V. Naumann et al., Solar Energy Materials and Solar Cells Vol. 120 (2014), 383-389

- Lock-in EBIC system by point electronic

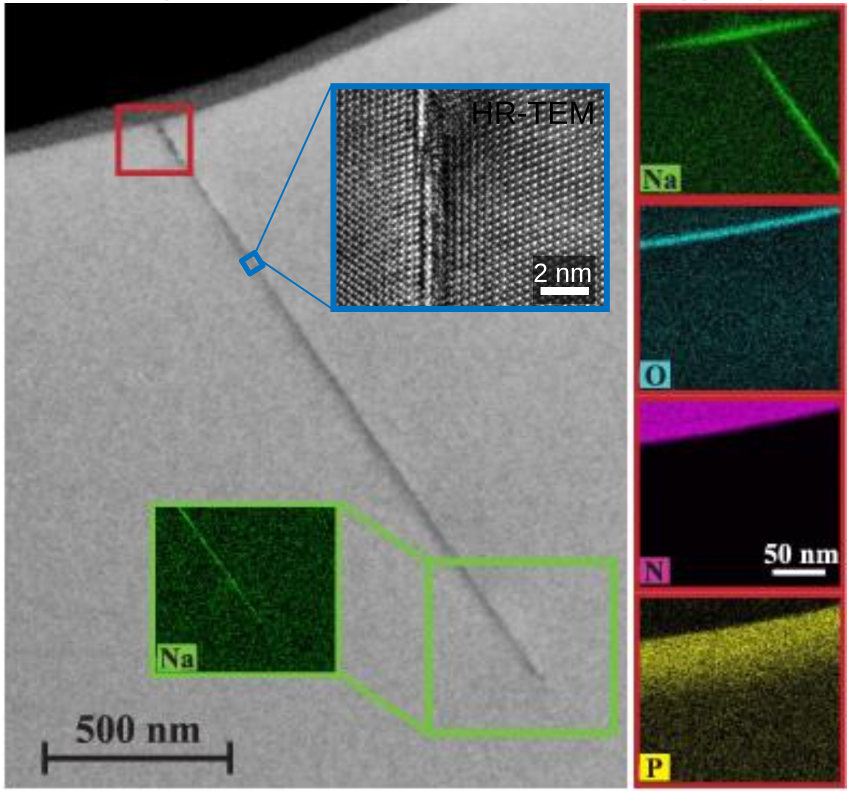
point electronic Fraunhofer CSP

Physical nature of PID-shunts: cross section

FIB cross section of a PID-shunt:



TEM image of a stacking fault + EDX mapping:

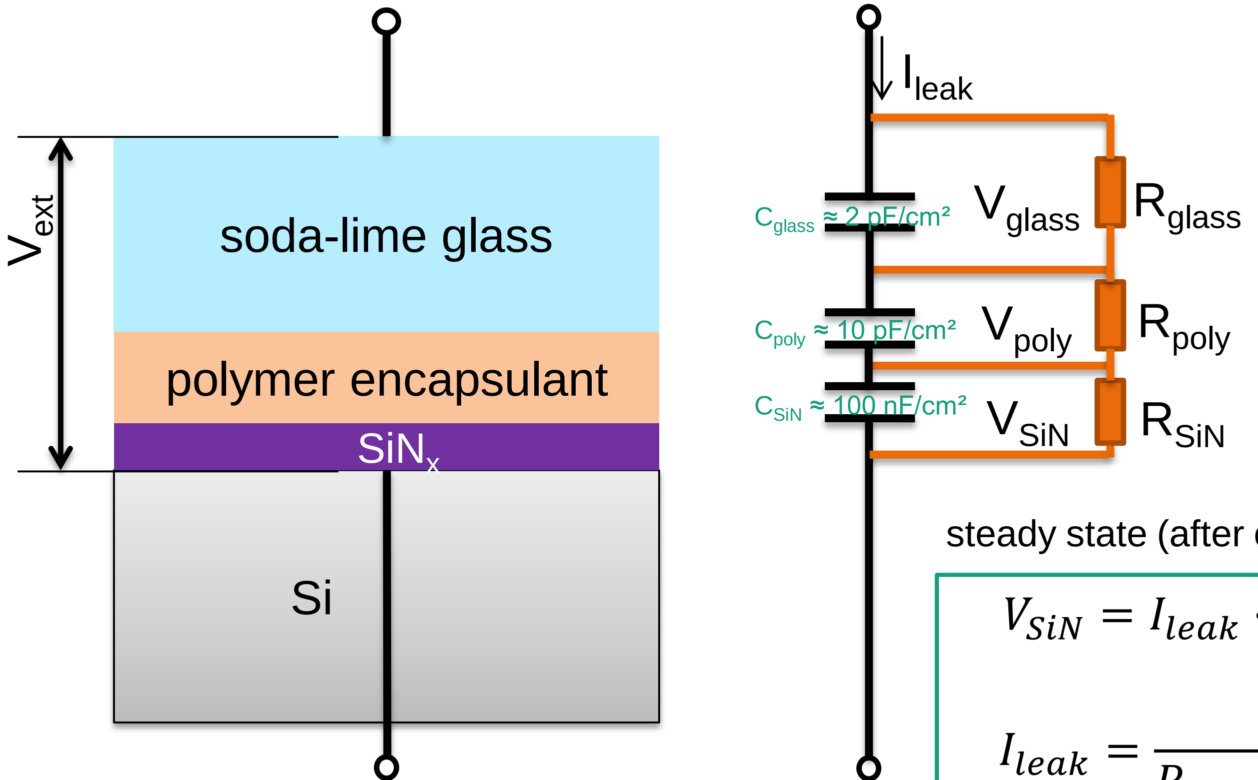


- PID-shunt = 2D crystal defect (“stacking fault”) in Si, decorated with Na [1]
- Corona test → Na comes from the surface of the cell, not from the glass
- Assumption: voltage across SiN_x antireflective layer critical for Na^+ ion drift

[1] V. Naumann et al., Solar Energy Materials and Solar Cells Vol. 120 (2014), 383-389

Voltage divider model for PID

Voltage divider model for PID on module level



steady state (after charging of all capacitors):

$$V_{SiN} = I_{leak} \cdot R_{SiN}$$

$$I_{leak} = \frac{V_{ext}}{R_{glass} + R_{poly} + R_{SiN}}$$

$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$

- Critical parameter for resistance against PID: voltage across SiN_x layer (V_{SiN})

[1] V. Naumann et al.: On the discrepancy between leakage currents and potential-induced degradation of crystalline silicon modules, *Proc. 28th European Photovoltaic Solar Energy Conference and Exhibition,* 2013, pp. 2994-2997

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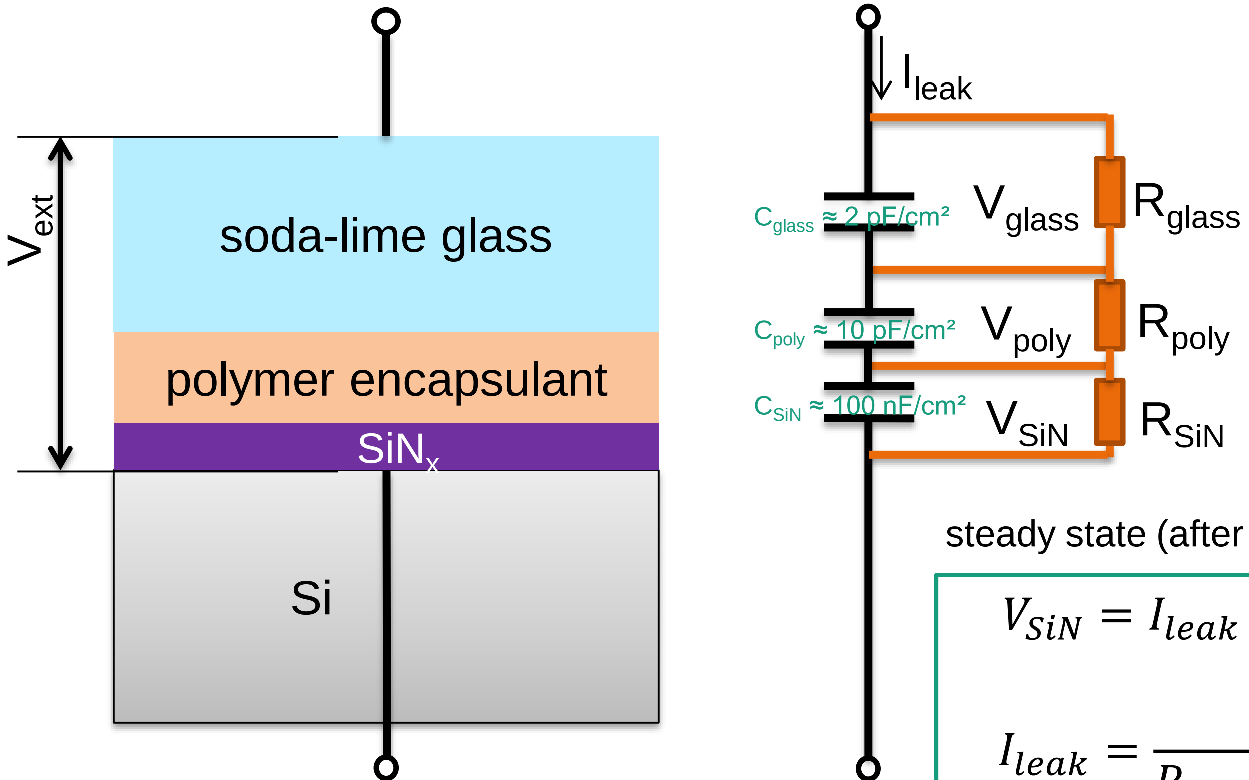

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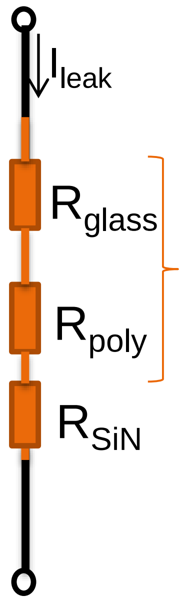
Voltage divider model

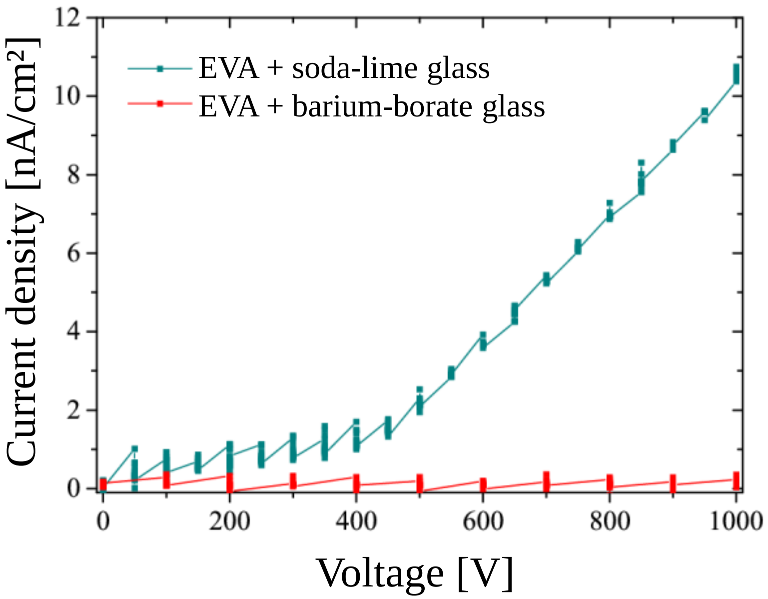
Case 1: control of the leakage current

$$V_{SiN} = I_{leak} \cdot R_{SiN}$$

- Reduced leakage current avoids PID-s
- Can be achieved through high resistance of encapsulation glass or polymer



$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$



Measurement of leakage current for different glass

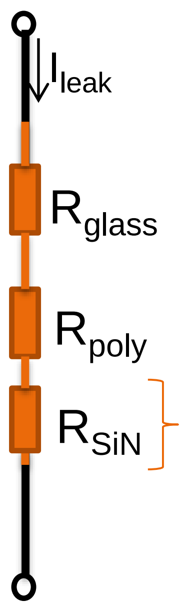
[1] V. Naumann et al., *Proc. 28th European Photovoltaic Solar Energy Conference and Exhibition,* 2013, pp. 2994-2997

Voltage divider model

Case 2: control of the SiN_x properties

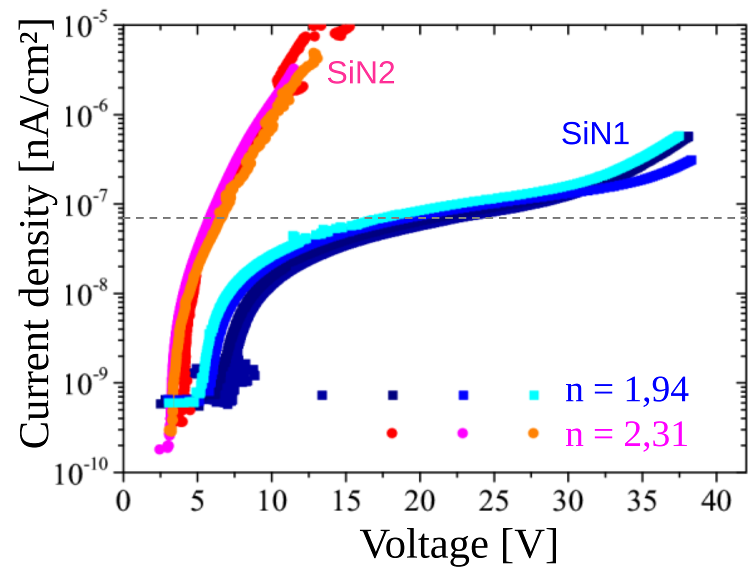
$$V_{SiN} = I_{leak} \cdot R_{SiN}$$

- Properties of SiN_x layer have no influence on the leakage current, but on the PID-s sensitivity
- Low resistivity of SiN_x at fixed leakage current gives reduced V_{SiN} and therefore less Na^+ ion drift across the SiN_x layer → avoids PID-s



SiN_x layer	refractive index	Si/N ratio	electronic conductivity	PID sensitivity
SiN1	1.93	low	low	high
SiN2	2.32	high	high	low

$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$



Measurement of the voltage across SiN_x layer

[1] V. Naumann et al., *Proc. 28th European Photovoltaic Solar Energy Conference and Exhibition,* 2013, pp. 2994-2997

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Approaches for preventing PID(-s)

Explanation with voltage divider model

$$V_{SiN} = \frac{R_{SiN}}{R_{glass} + R_{poly} + R_{SiN}} V_{ext}$$

System level	
▪ Avoid high negative bias of cells in modules [1]	$V_{ext} \rightarrow 0$ → $I_{leak} \rightarrow 0$ → $V_{SiN} \rightarrow 0$
Module level	
▪ Front glass with less mobile ions (quartz glass) [2]	$R_{glass} \uparrow$ → $I_{leak} \downarrow$ → $V_{SiN} \downarrow$
▪ Encapsulants with reduced mobility of ions [1, 2]	$R_{poly} \uparrow$ → $I_{leak} \downarrow$ → $V_{SiN} \downarrow$
Cell level	
▪ Low potential across SiN_x layer through increased conductivity (refractive index ↑ [1, 3], doping [4])	$R_{SiN} << R_{glass} + R_{poly}$, $R_{glass} + R_{poly} = const.$ → $I_{leak} = const.$, $R_{SiN} \rightarrow 0$ → $V_{SiN} \rightarrow 0$
▪ Modification of the Si surface before SiN_x deposition [5]	presumably not electrical effect

[1] S. Pingel et al., in: Proc. 35th IEEE Photovoltaic Specialists Conference, USA, 2010, pp. 2817–2822.
[2] P. Hacke et al., in: Proceedings 37th IEEE PVSC, Seattle, WA, USA, 2011, pp. 814–820.
[3] H. Nagel et al., in: Proceedings 26th EUPVSEC, Hamburg, Germany, 2011, pp. 3107–3112.
[4] Patent DE 10.2010.017.461.A1 2011.12.22.
[5] H. Mehlich et al., in: Proceedings 27th EUPVSEC, Frankfurt, Germany, 2012, pp. 3411–3413.

Conclusion

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- PID cell test provides economic PID testing of solar cells and encapsulants
- PID-s: stacking faults in Si become conductive by decoration with Na
- PID degradation rate and final condition depend on voltage in the SiN_x layer, which is a function of leakage current and SiN_x layer's electronic conductivity

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GEFÖRDERT VOM

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